Insertion Strategy for EUV Lithography Timing & Risks with HVM

Pawitter Mangat

GLOBALFOUNDRIES

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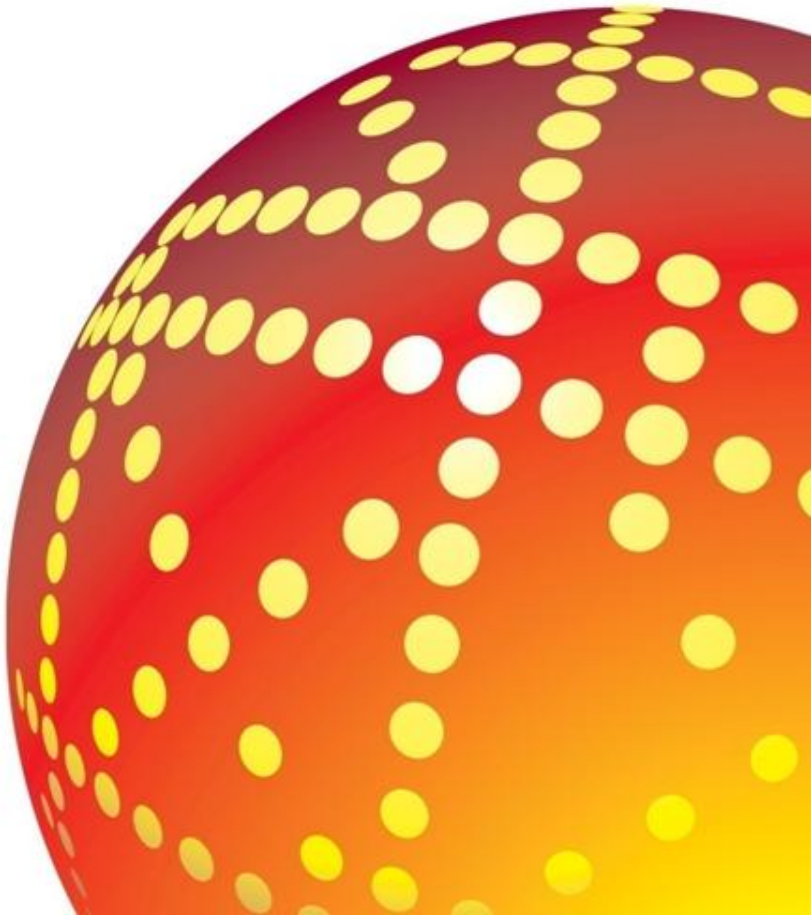
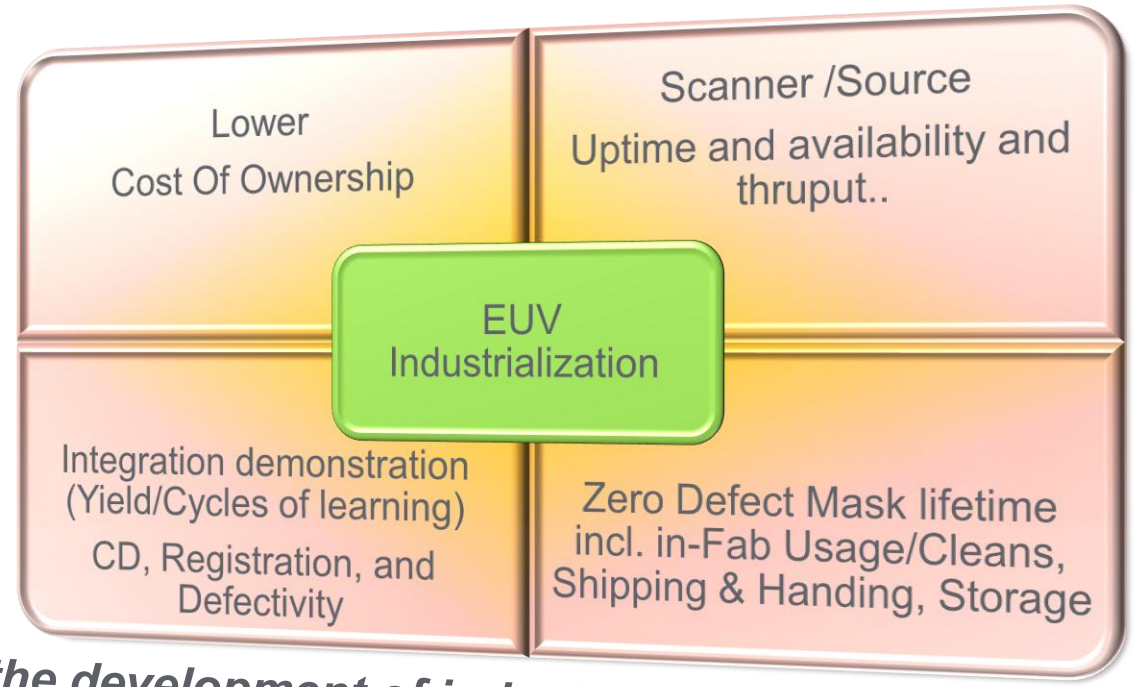


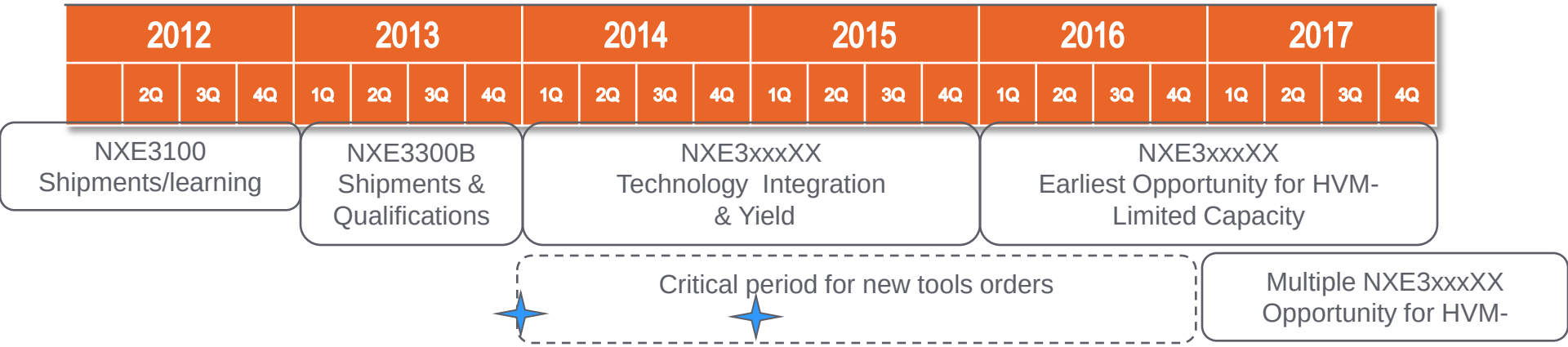
Outline of Presentation

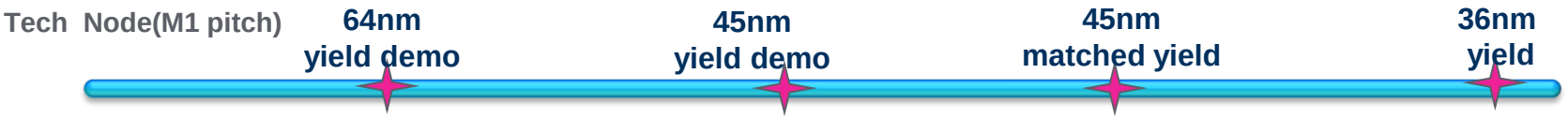
- EUV HVM Insertion Timing, Thruput and Device type
- EUV Eco System Requirements
- EUVL Scaling path
- Summary



the development of industry on an extensive scale

EUV -Tools





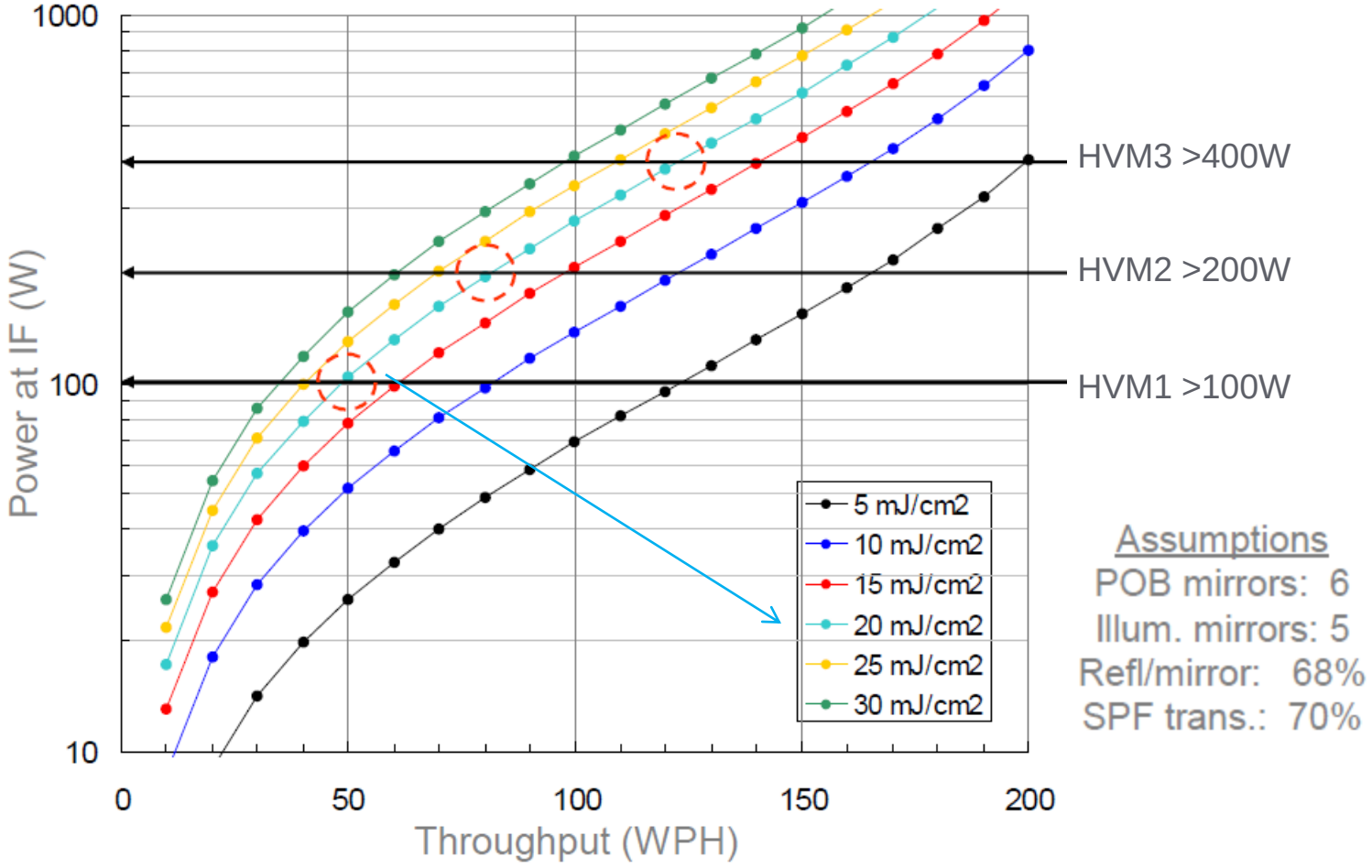
EUV Source Power is the Foundation for HVM

Cymer, SPIE, 2012 EUV Source Power Roadmap

Source Model	HVM I	HVM II	HVM III
Average Laser Power (kW)	13	29	31
In-band CE (%)	3.0	3.5	4.0
Collection Efficiency (%)	24	19	21
Clean EUV Power (W)	**105**	**250**	**350**

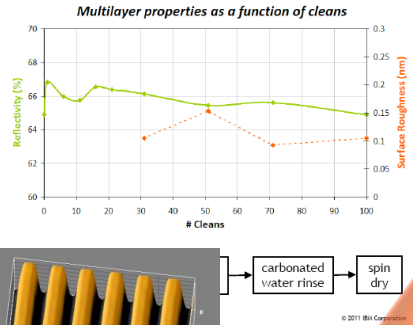
- EUVL will likely be used first for contact and via levels.
  - Single exposure, low pattern density(Defect avoidance via pattern shifting) and better imaging
- Followed by use for cut-mask exposures & back-end metal levels patterning.
  - Single exposure and better imaging (less corner rounding and smaller tip-to-tip distances)

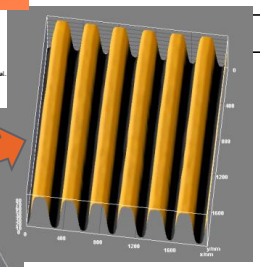
EUV Power and Thruputs

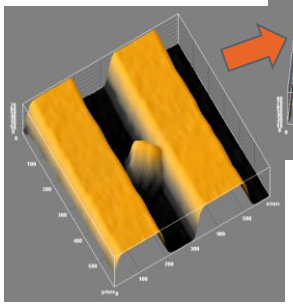


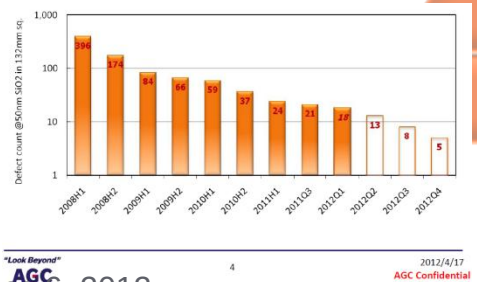
Masks for EUV?

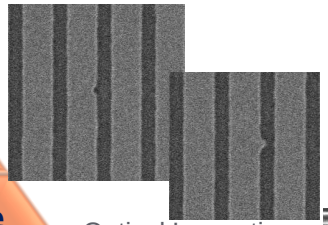
- Zero defect printability needs a lot of Mask supporting infrastructure

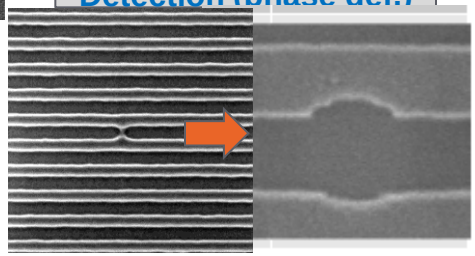












HVM

Storage

Mask Lifetime

Mask in-Use & Handling

Defect Free S&H

Inspection, Repair and Phase Defect compensation

Absorber patterning process with black border

Defect mitigation by pattern shift/ blank rotation

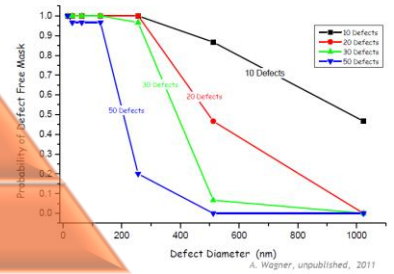
Low defect mask blanks with Fiducials (Location accuracy)

Optical Inspection @ 40nm sensitivity

No Mask Blank Def. Detection (phase def.)

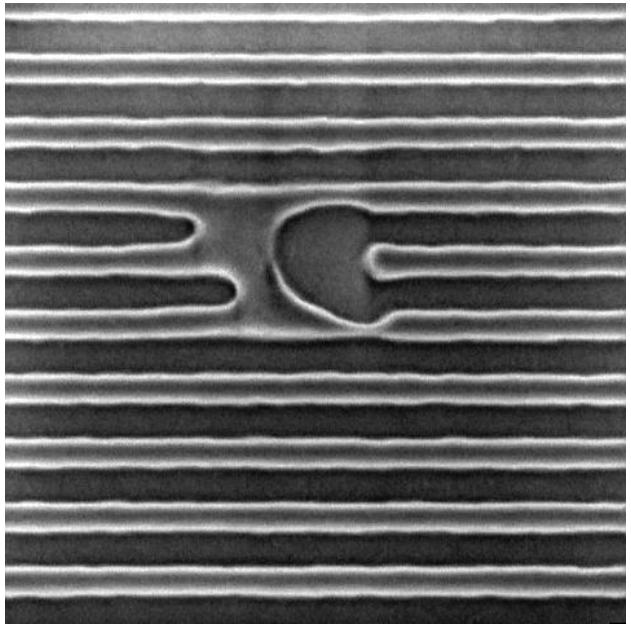
Defect avoidance: pattern shift

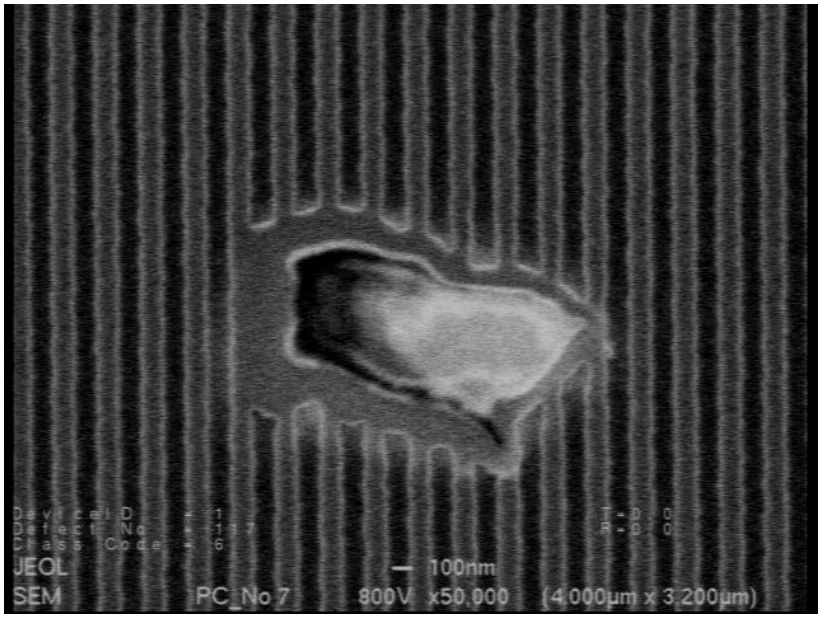
- Explore the effect of blank defects on mask yield with pattern shift on the same contact design data
  - Up to 16um pattern shift in x or y
- *Large defects will impact yield*
- *~30 defects is the upper limit for reasonable yield*
- Feasible!



Masks for EUV?

- What keeps me awake?—Killer Blank defects
  - non –repairable
  - Impacts Pattern Shift
  - And more…

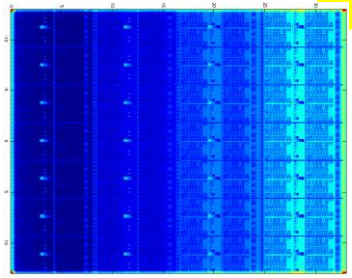




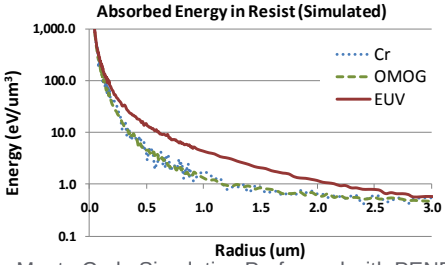
OPC for EUV?

- EUV scanner resolution makes conventional OPC trivial
  - k1 < 0.5 for 32nm pitch node
- But, new effects related to inability of materials to absorb, reflect or refract light well at 13.5nm cause non-idealities that must be corrected by OPC
- Sources of EUV OPC Error
  - Flare
  - Horizontal vertical print differences
  - Systematic mask errors due to electron backscatter that are not corrected during mask writing
- Conventional optical proximity correction methods are applicable for EUV, but additions are essential to the OPC flow to correct for new effects.
  - Exploit design hierarchy to improve runtime and file size(flare)

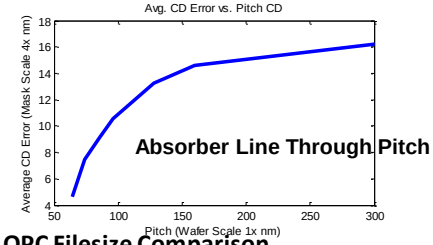
Pitch (nm)	Wavelength (nm)	NA	k1
144	193	1.35	0.50
64	13.5	0.25	0.59
56	13.5	0.25	0.52
45	13.5	0.33	0.55
32	13.5	0.33	0.39

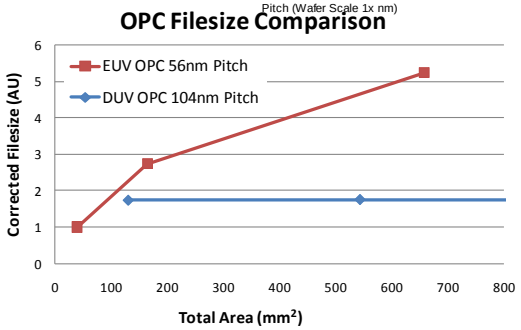


Clifford, SPIE 2012



Monte Carlo Simulation Performed with PENELOPE



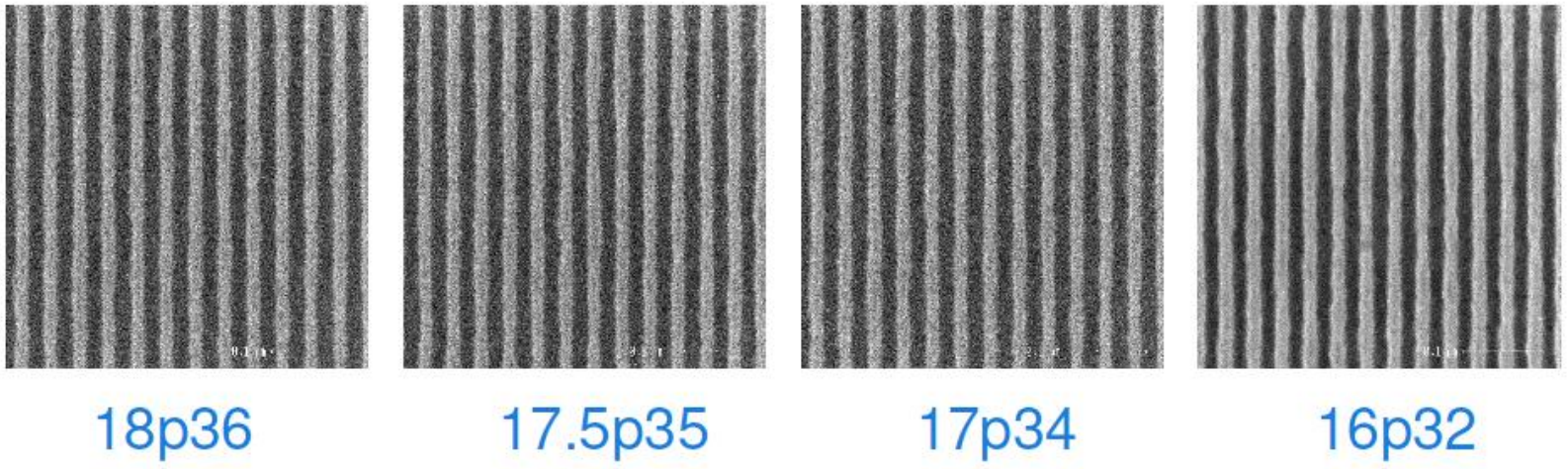


Overlay for EUV?

Year of production	2012	2013	2014	2015	2016	2017	2018
Overlay (3 sigma) (nm)	6.4	5.4	4.8	4.2	3.8	3.4	3

- Tight overlay Spec. but additional challenges associated with EUV
  - Lens heating
  - Other thermal challenges due to vacuum
  - Reticle non-flatness
  - Higher levels of aberrations

Resists for EUV?

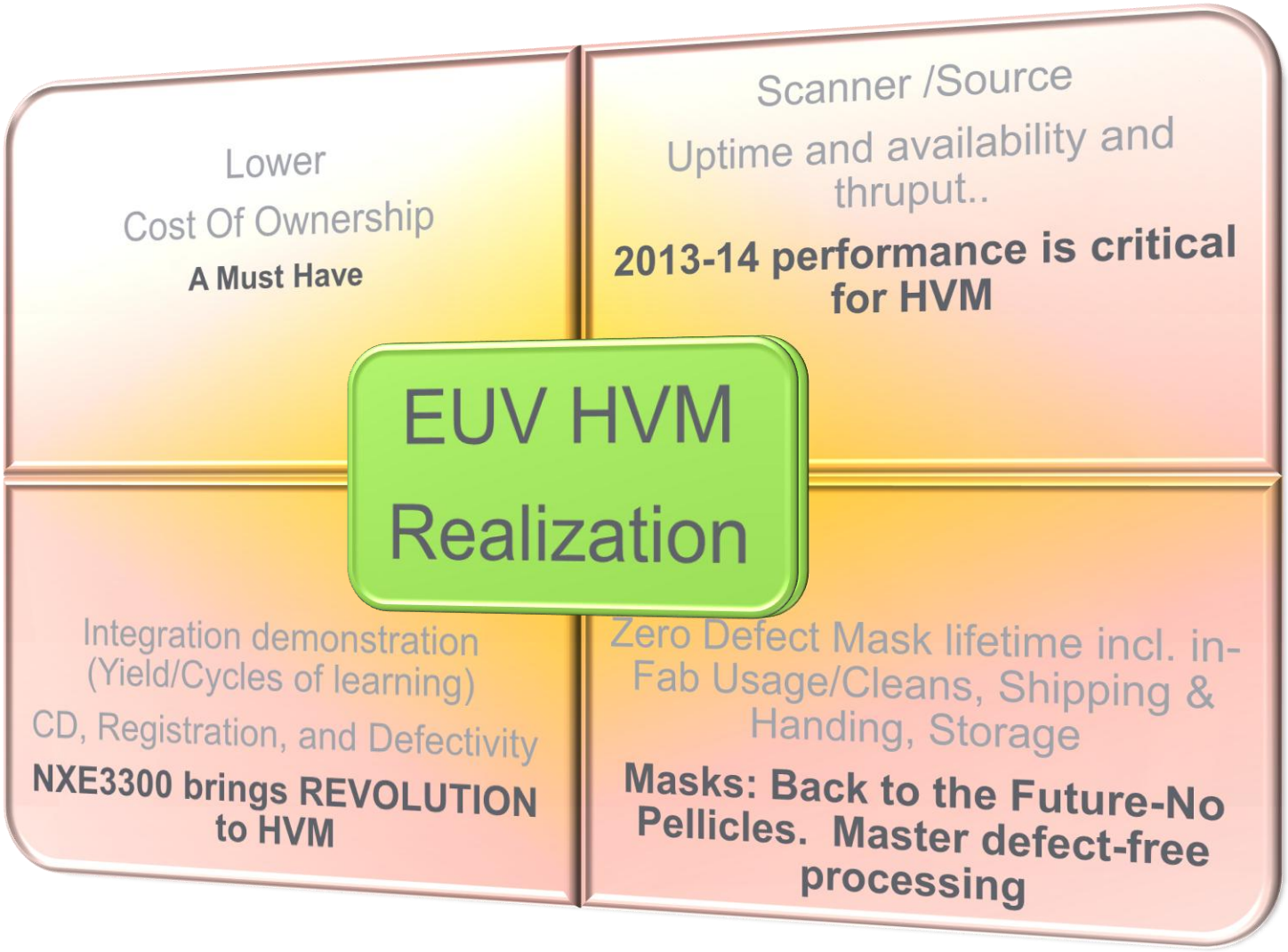


- Resolution is more-than adequate for initial foundry process where EUV would provide benefit.
- LER still needs improvement.
- Contact hole resolution needs to be improved.

EUV for future nodes?

- We Need EUV HVM NOW!..Pilot line efficiencies by 2015
- When EUV lithography works
  - Then, Double patterning using EUV might be an option
- If EUV doesn't work,
  - then scaling will slow down
  - And, Triple-patterning….Very expensive option, Not well received by market (Foundry Customers)
- Options for Future
  - Directed Self Assembly… Defectivity and integration?.
  - MBDW on 450mm …Thruput.?.
  - 13.53nm must work.. Let's talk higher NA before wavelength change(6.x)
  - Innovations…Always an Option!!!

Summary


Lower
Cost Of Ownership
A Must Have
Scanner /Source
Uptime and availability and thruput..
2013-14 performance is critical for HVM
EUV HVM Realization
Integration demonstration (Yield/Cycles of learning)
CD, Registration, and Defectivity
NXE3300 brings REVOLUTION to HVM
Zero Defect Mask lifetime incl. in-Fab Usage/Cleans, Shipping & Handing, Storage
Masks: Back to the Future-No Pellicles. Master defect-free processing

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